CLAIMS

What is claimed is:

1. A method of generating a nanostructure, the method comprising the steps of:

depositing on a surface of a substrate a plurality of layers at least one of which is a tunable etch resistant anti-reflective (TERA) layer;

patterning through the TERA layer;

oxidizing a remaining portion of the TERA layer to generate an oxidized TERA layer; and

generating the nanostructure in the plurality of layers using the oxidized TERA layer as a mask.

2. The method of claim 1, wherein the plurality of layers includes a polysilicon layer on the surface, a silicon nitride layer on the polysilicon layer, the TERA layer on the silicon nitride layer, and a photoresist on the TERA layer.

3. The method of claim 2, wherein patterning step includes imaging the photoresist layer and removing an exposed area of the TERA layer.

4. The method of claim 3, further comprising the step of etching the photoresist layer to trim an image in the photoresist layer prior to removing the exposed area of the TERA layer.

5. The method of claim 2, wherein the nanostructure generating step further includes using the oxidized TERA layer as a mask for etching of the nitride and polysilicon layers, and stripping the oxidized TERA layer.

6. The method of claim 1, wherein the nanostructure has a surface roughness of no greater than approximately 4.0 nm rms.

7. The method of claim 1, wherein the nanostructure generating step includes trimming the oxidized TERA layer with neutral molecules from a gaseous hydrogen fluoride/ammonia mixture.

8. The method of claim 1, wherein the oxidizing step includes oxidizing in a plasma at approximately 250° C, and includes removal of a photoresist layer.

9. The method of claim 1, wherein the TERA layer includes carbon, hydrogen, oxygen and silicon, and the oxidized TERA layer consisting essentially of oxygen and silicon.

10. A method of enhancing optical properties and etch selectivity during nanostructure fabrication, the method comprising the steps of:

depositing a tunable etch resistant anti-reflective (TERA) layer including carbon, hydrogen, oxygen and silicon;

patterning the TERA layer as a mask for etching; and

enhancing etch selectivity to silicon nitride by oxidizing the TERA layer to form an oxidized TERA layer consisting essentially of oxygen and silicon.

11. The method of claim 10, wherein the depositing step includes depositing on a surface of a substrate a plurality of layers including a polysilicon layer on the surface, a silicon nitride layer on the polysilicon layer and the TERA layer on the silicon nitride layer;

patterning the TERA layer; and

wherein the method further comprises the step of:

generating a nanostructure in the silicon nitride layer and the polysilicon layer using the oxidized TERA layer as a mask.

12. The method of claim 10, wherein patterning step includes:

depositing a photoresist on the TERA layer;

photolithographically printing to generate a photoresist mask; and

removing an exposed area of the TERA layer.

13. The method of claim 12, further comprising the step of etching to trim the photoresist mask.

14. The method of claim 10, further comprising the step of trimming the oxidized TERA layer with neutral molecules from a gaseous hydrogen fluoride/ammonia mixture.

15. The method of claim 14, wherein the gate generating step further includes at least one etching of the silicon nitride layer and the polysilicon layer using the oxidized TERA layer as a mask.

16. The method of claim 10, further comprising the step of stripping the oxidized TERA layer using wet oxide etch chemistry.

17. The method of claim 10, wherein the oxidizing step includes oxidizing in a plasma at approximately 250° C.

18. A nanostructure comprising:

a plurality of layers, at least one of which is an oxidized tunable etch anti-reflective (TERA) layer.

19. The nanostructure of claim 18, wherein the plurality of layers includes a polysilicon layer on a surface of a substrate, a silicon nitride layer on the polysilicon layer and the TERA layer on the silicon nitride layer.

20. The nanostructure of claim 18, wherein the nanostructure has a surface roughness of no greater than approximately 4.0 nm.